CLAIMS

Please **CANCEL** claims 1-15 as follows:

A status of the claims is provided below.

16. (original) A method of fabricating a varactor, comprising:

providing a semiconductor substrate;

doping a lower region of the semiconductor substrate with a first dopant;

doping a middle region of the semiconductor substrate with a second dopant; and

doping an upper region of the semiconductor substrate with a third dopant.

17. (original) The method of claim 16, further comprising forming a cathode of the varactor in the lower region, forming a hyper-abrupt junction in the middle region, and forming an anode in the upper region.

18. (original) The method of claim 16, further comprising forming the first dopant from a first N- type dopant, forming the second dopant from a second N-type dopant, and forming the third dopant from a P-type dopant.

19. (original) The method of claim 16, further comprising doping a bottom layer of the lower region with a higher concentration of the first dopant than an upper layer of the lower region.

20. (original) The method of claim 19, further comprising forming a collector of the varactor in the upper layer of the lower region of the semiconductor substrate.

21. (original) The method of claim 16, further comprising forming at least one isolation region adjacent to the lower, middle, and upper regions of the semiconductor substrate.

22. (original) The method of claim 16, further comprising forming at least one reach-through implant in electrical communication with the lower region of the semiconductor substrate.

23. (original) The method of claim 16, further comprising forming a silicided layer on a top of the semiconductor substrate above the upper region.